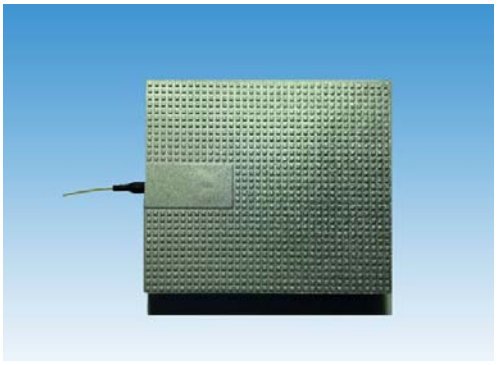
40Gb/s 300 Pin MSA compliant Receiver module

GR3T1LL

Features



- 40G 300 PIN MSA compliant
- Support VSR2000-3R1 and VSR200-3R2
- Support OC-768/STM-256 (39.813Gbps) to G.709/OTU3 (43.018Gbps)
- NRZ-Modulation
- 16 x 2.5Gb/s CML electrical interface and compliant with OIF SFI-5.1 standard
- Provide MSA 40G I^2C interface for control, monitoring, and alarms
- +3.3V,+5V,-5.2V power supply
- Typical power consumption of 4.5W
- Operating case temperature: -5 to 70 ℃
- Standard LC/PC connector
- 3.2” x 2.7” x 0.55” small form factor
- ROHs-6 compliant

Applications

- Internet Security & Monitor Systems
- High Speed Telecom & Data Communication

Description

GR3T1LL is the industry’s smallest and most advanced 40Gb/s 300 pin MSA compliant Rx module for VSR2000 applications. A 1310/1550nm compatible PIN based low-noise receiver is incorporated to receive NRZ coding optical signal. A set of advanced Demux IC translate the OC-768, STM-256, or G.709 data stream to a SFI-5 compliant high-speed CML output, allowing direct connection to a framer or a FEC IC on the line card.

The Rx module's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Internet security and monitoring applications.

The Rx module is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

Product Selection

GR3T1LL

G: GWorld
R: Receiver
T1: Transponder Solution 1
L: LC/PC connector
L: Large Form Factor

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1 Features

GR3T1LL is the industry's smallest and most advanced 40Gb/s 300 pin MSA compliant Rx module for VSR2000 applications. A 1310/1550nm compatible PIN based low-noise receiver is incorporated to receive NRZ coding optical signal. A set of advanced Demux IC translate the OC-768, STM-256, or G.709 data stream to a SFI-5 compliant high-speed CML output, allowing direct connection to a framer or a FEC IC on the line card.

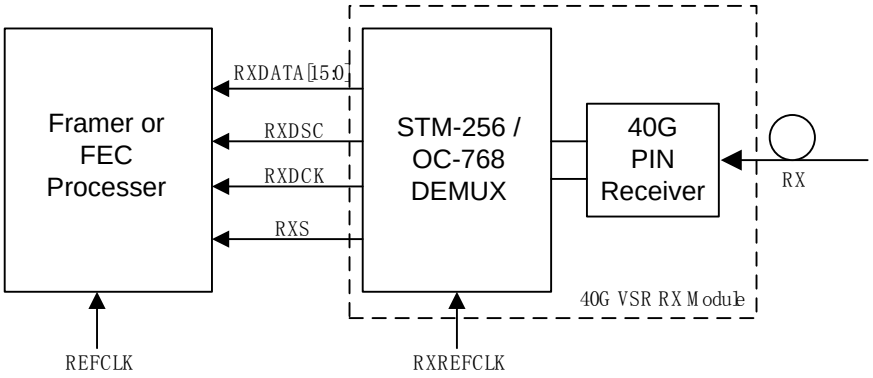

Figure 1 SFI-5 Interface

- Compliant with MSA Agreement《REFERENCE DOCUMENT FOR 300 PIN 40Gb TRANSPONDER》;
- Support VSR2000-3R1 and VSR200-3R2
- Support OC-768/STM-256 (39.813Gbps) to G.709/OTU3 (43.018Gbps);
- 16 lanes of 2.5Gb/s high-speed CML electrical interface and compliant with OIF SFI-5.1 standard;
- Software interface is compliant to 《MSA 10G/40G TRX I2C Public Document 04 Final》 for control, monitoring, and alarms for optics management;
- Standard LC/PC connector;
- 1310~1550nm wide range wavelength PIN receiver on receiver side;
- Power consumption of 4.5W typical and 6W maximum;
- 3.2" x 2.7" x 0.55" (79.9 x 68.6 x 14.0 mm);

2 Hardware Specifications

2.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max	Unit
Storage Temperature (case)	T_{stg}	—	-40	+85	C
Relative Humidity	RH	—		85	%
Receiver Optical Power	Pmax	—		+3.5	dBm
Power Supply	+5.0V	—	-0.5	+6.0	V
	+3.3V	—	-0.5	+4.0	V

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	-5.2V	—	-0.5	-6.0	V
Input LVTTL and LVCMOS Signal Level	Vio	—	-0.5	+3.6	V
Minimum Fiber Bend Radius	Rbend	—	30		mm
ESD Sensitivity	HBM	Human Body model R=1.5K, C=100pF	—	2000	V

2.1 Recommended operating conditions

Table 2 Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	Top	-5	—	+70	C
Operating wavelength	λ	1530	—	1565	nm
Supply Voltage	$V_{+5.0V}$	+4.75	+5.0	+5.25	V
	$V_{+3.3V}$	+3.14	+3.3	+3.47	V
	$V_{-5.2V}$	-4.95	-5.2	-5.5	V
	V_{APS}	—	Not Used	—	V
Supply Current	$I_{+5.0V}$	—	0.1	0.2	A
	$I_{+3.3V}$	—	0.4	0.6	A
	$I_{-5.2V}$	—	0.7	1.0	A
	I_{APS}	—	Not Used	—	A
Power dissipation	P	—	4.5	6.0	W
Link Distance	L	0	—	2km	G.652 SMF
Application		40Gbps VSR2000 3R1 3R2			

3 Optical Specifications

Table 3 Optical Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Receiver							
Wavelength Range	△λ		1250	1550	1580	nm	
Data Rate	F_{DATA}		39.8	—	43.1	Gbps	
Sensitivity @ 1550nm		BER=10^{-12} ER=8.2	—	-10.0	-9.0	dBm	1
Sensitivity @ 1310nm		BER=10^{-12}	—	—	-7.0	dBm	
Receiver Overload			+3.0	—	—	dBm	
Optical Path Penalty			—	—	2.0	dBm	2
Optical Return Loss	R_L		27	—	—	dB	
Jitter Charateristics			Compliant with ITU-T G.8251				

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Note1: Life beginning test data, receive sensitivity is guarantee in 39.813Gbps, and will have some degrade in 43.018Gbps application.

Note2: Optical path penalty is tested in 2km G.652 SM fiber link

4 Electrical Specifications

The SFI-5 data interface is defined to be a 1.2V CML as described in OIF2001.149.X. The transponder is both AC and DC compliant (drivers and receivers will support both AC and DC coupling). There will be no DC blocking capacitors inside the transponder data lines. If AC coupling is required for operation, the customer is expected to implement the DC blocking capacitors on the line card.

Table 4 SFI5 CML Signal Output Characteristics (DC coupled inside the module)

Parameter	Symbol	Min	Max	Unit	Condition
Differential CML Output Signals	1.2V Referenced (SFI5 Output Signal)				
Output Voltage (Diff Vpp)	VDF	0.6	1	V	2.5Gbps
Single ended Output impedance	RSE	35	65	Ohm	at DC
Differential Output Impedance	RD	75	125	Ohm	at DC
Differential Return Loss	RLDIFF	10		dB	<3.0GHz
Single Ended Return Loss	RLSE	10		dB	<3.0GHz
Output Short Circuit Currents	IDSHORT	50	50	mA	
Clock Duty Cycle		40	60	%	
Output Common mode Voltage		0.72	1.23	V	
Rise/Fall Time	TR/TF	50	120	ps	20% ～ 80%
RxDATA skew to RxDSC	TSKEW	100	100	ps	

Table 5 Reference Clock (AC coupled inside the module)

Parameter	Symbol	Min	Typ	Max	Unit
RXREFCK Frequency	FRXREF	-100ppm	$f_{DATA}/16$ or $f_{DATA}/64$	+100ppm	MHz
RXREFCK Jitter	TJ			1.8	ps (RMS)
RXREFCK Input common mode	VCM-RXREF	-0.1		+0.1	V
RXREFCK Duty Cycle	DCRXREF	45		55	%
RXREFCK Rise/Fall Time @ fDATA/16	TR/TF	50		103	ps

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RXREFCK Rise/Fall Time @ fDATA/64	TR/TF	50		411	ps
RXREFCK Level (SingleEnded)	VRXREFCK	450		1100	mVpp

Table 6 Rx Monitor Clock (AC coupled inside the module)

Parameter	Symbol	Min	Typ	Max	Unit
Signal Type	CLM compatible, ground referenced				
RXMONCLK Frequency	fRXMONCLK	-100ppm	f_{DATA} /64	+100ppm	MHz
RXMONCK Input common mode	VCM	160		240	mV
RXMONCK SingleEnded Level	VSE	320		480	mVpp

5 Electrical Interface

5.1 Internal reference structure

The internal structure of GR3T1LL is shown as Figure 2.

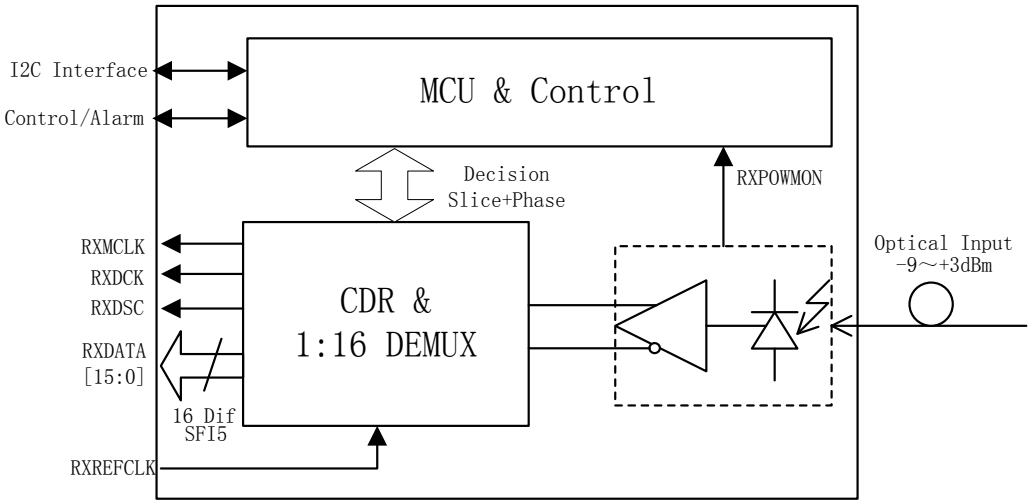

Figure 2 Internal Structure

5.2 Pin Definitions

GR3T1LL hardware connector is compliant with MSA300 agreement and pin definitions are listed in Table 7. Tx pin is useless and left open in module.

Table 7 Pin Definitions

	K	J	H	G	F	E	D	C	B	A
1	Digital GND	RxDSCP	Digital GND	RxData12P	Digital GND	RxData8P	Digital GND	RxData4P	Digital GND	RxData0P
2	Digital GND	RxDSCN	Digital GND	RxData12N	Digital GND	RxData8N	Digital GND	RxData4N	Digital GND	RxData0N
3	THRESH_A	Digital GND	-5.2V Digital	Digital GND	FFU	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
4	Digital GND	RxDCKP	Digital GND	RxData13P	Digital GND	RxData9P	Digital GND	RxData5P	Digital GND	RxData1P

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5	Digital GND	RxDCKN	Digital GND	RxData13N	Digital GND	RxData9N	Digital GND	RxData5N	Digital GND	RxData1N
6	LOS	Digital GND	-5.2V Digital	Digital GND	IIC ADDR_0	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
7	Digital GND	RxREFCKP	Digital GND	RxData14P	Digital GND	RxData10P	Digital GND	RxData6P	Digital GND	RxData2P
8	Digital GND	RxREFCKN	Digital GND	RxData14N	Digital GND	RxData10N	Digital GND	RxData6N	Digital GND	RxData2N
9	FFU	Digital GND	-5.2V Digital	Digital GND	IIC_ADDR_	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
1	IIC_SDA	FFU	Digital GND	RxData15P	Digital GND	RxData11P	Digital GND	RxData7P	Digital GND	RxData3P
1	Digital GND	RxMONCK	Digital GND	RxData15N	Digital GND	RxData11N	Digital GND	RxData7N	Digital GND	RxData3N
1	IIC_SCL	Digital GND	RXS	Digital GND	IIC_ADDR_	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
1	FFU	MCU_RST	DSP_TCK	DSP_TMS	DSP_TDO	DSP_TDI	APS Sence	RTCK	ISP_EN	FFU
1	Analog	-5.2V	Analog	-5.2V	Analog	3.3V Analog	Analog	3.3V Analog	Analog	5.0V Analog
1	Analog	-5.2V	Analog	-5.2V	Analog	3.3V Analog	Analog	3.3V Analog	Analog	5.0V Analog
1	Analog	-5.2V	Analog	-5.2V	Analog	3.3V Analog	Analog	3.3V Analog	Analog	5.0V Analog
1	FFU	TDO	TDI	TCK	TMS	NTRST	APS Set	RXD	TXD	FFU
1	Digital GND	NC	FFU	FFU	Digital GND	FFU	FFU	FFU	FFU	FFU
1	NC	Digital GND	-5.2V Digital	Digital GND	CFG_ALM	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
2	STAT_INT	Digital GND	-5.2V Digital	Digital GND	NC	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
2	REG_RESE	Digital GND	-5.2V Digital	Digital GND	APS Digital	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
2	MOD_RESE	Digital GND	-5.2V Digital	Digital GND	APS Digital	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
2	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC
3	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC	Digital GND	NC

Differential data / Clock Signals

Power Pins

Ground Pins

Control Signals

NUC no user connection /

FFU: reserved for future use

NC: no connection in module (Preseve for Tx

5.3 Pin Description

Pin description of GR3T1LL is listed according to function.

Table 8 RX SFI-5 High Speed Signal Interface

Pin	Name	Levels	I/O	Description	Default
See MSA300	RXDATAP/N [15:0]	Diff CML	O	Receive Data Bus SFI5 compliant 16 wide receive data bus from SerDes	data rate/16
J1 J2	RXDSCP/N	Diff CML	O	Receive Deskew channel used to deskew the RX_DATA[15:0]	data rate/16
J4 J5	RXDCKP/N	Diff CML	O	Receive Data Clock provides a timing reference for receive data. It is at ¼ data rate of RXDATA and RXDSC	data rate/64

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J7 J8	RXREFCKP/N	AC Coupled LVPECL	I	Receive Reference Clock provides an alternate timing reference. The clock is at ¼ data rate of RXDATA and RXDSC	data rate/64
J11	RXMONCK	Analog	O	Receive Monitor Clock provides a single ended clock that can be used to monitor the receive clock on the demux. This clock shall be turned off during normal operation and startup.	data rate/64

Table 9 Alarms

Pin	Name	Levels	I/O	Description	Default
H12	RXS	LVCMOS	O	Receiver Status is an asynchronous signal used to indicate an alarm to the Framer (active high).	0
K6	LOS	LVCMOS	O	Loss of Signal is a signal to indicate to the there is no incoming optical signal (active low).	1
K22	STAT_INT	LVCMOS	O	Status Interrupt is an electrical “or” of the status register (active low).	1
F19	CFG_ALM	LVCMOS	O	User Configurable Alarm is a user selectable alarm pin. TBD Alarm signals can be software configured to this pin.	1

Table 10 Digital and Analog Control Signals

Pin	Name	Levels	I/O	Description	Default
K3	THRESH_ ADJ	Analog	I	Threshold Adjust is a signal used to control the receive signal threshold. This feature is shall be supported through I2C and the THRESH_ADJ pin suggested left open or connect to 1.25V Reference.	1.250V
K25	REG_RES ET	LVCMO S	I	Register Reset is active low and when asserted to its low state will return all writable registers to their default state after resetting the MCU/FPGA on the transponder.	1

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K28	MOD_RESET	LVCMOS	I	Module Reset is active low and when asserted to its low state will reset the optical module. The module reset will force all components in the transponder to their reset state, including the I2C registers, the laser and the respective chips.	1

Table 11 I2C Interface

Pin	Name	Levels	I/O	Description	Default
F6	I2CADDR0	LVTTL	I	Address line A0, A1, A2 for serial interface (internal 10kohm pulldown)	0
F9	I2CADDR1	LVTTL	I		0
F12	I2CADDR2	LVTTL	I		0
K10	I2C_SCL	Open collector	I/O	Serial interface clock (internal 10kohm pulldown)	1
K12	I2C_SDA	Open collector	I/O	Serial data line (internal 10kohm pulldown)	1

Table 12 Power Supplies

Pin	Name	Levels	I/O	Description	Default
B3, B6, B9, B12, B19, B22, B25, B28	+3.3V Digital	V+3.3VD	I	+3.3VD supply	+3.3V
H3, H6, H9, H19, H22, H25, H28	+5.2V Digital	V-5.2VD	I	-5.2VD supply	-5.2V
C14, C15, C16, E14, E15, E16	+3.3V Analog	V+3.3VA	I	+3.3VA supply	+3.3V
A14, A15, A16	+5.0V Analog	V+5VA	I	+5.0VA supply	+5.0V
G14, G15, G16, J14, J15, J16	-5.2V Analog	V-5.2VA	I	-5.2VA supply	-5.2V
D3, D6, D9, D12, D19, D22, D25,D28, F25, F28	APS Digital	VAPS	I	MSA compliant APS	Not Used
A3, A6, A9, A12, A19, A22, A25, A28,B1, B2, B4, B5, B7, B8, B10, B11,B20, B21, B23, B24, B26, B27, B29,B30, C3, C6, C9, C12, C19, C22, C25,C28, D1, D2, D4, D5, D7, D8, D10,D11, D20, D21, D23, D24, D26, D27,D29, D30, E3, E6, E9, E12, E19, E22,E25, E28, F1, F2, F4, F5, F7, F8, F10,F11, F18, F20, F21, F23, F24, F26,F27, F29, F30, G3, G6, G9, G12, G19,G22, G25, G28, H1, H2, H4, H5, H7,H8, H10,	Digital Ground	GND	I	Digital Ground	0V

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H11, H20, H21, H23, H24,H26, H27, H29, H30, J3, J6, J9, J12,J19, J22, J25, J28, k1, K2, K4, K5, K7,K8, K11, K18, K20, K21, K23, K24,K26, K27, K29, K30					
B14, B15, B16, D14, D15, D16, F14,F15, F16, H14, H15, H16, K14, K15,K16	Analog Ground	GNDA	I	Analog Ground	0V

6 Software Interface

This module has I2C standard bus with two open collector or open drain SDA and SCL lines for software communication between line card and module. Software interface is compliant to 《MSA 10G/40G TRX I2C Public Document 04 Final》 for control, monitoring, and alarms for optics management. Because VSR Rx Module only has receiver function, some command related to transmit function is not supported.

Table 13 I2C Commands

Cmd (hex)	MSA	Prot.	Pin	Soft	Description
44	✓			✓	Set RX Command Register
45	✓			✓	Read RX Command Register
46	✓	🔒		✓	Save RX Command Register
47	✓	🔒		✓	Restore RX Command Register
4B	✓	🔒		✓	Set Receive Decision Threshold
4C	✓		✓	✓	Read Receive Decision Threshold
4D		🔒			Set Demux Phase Offset
4E					Read Demux Phase Offset
4F					Set Configurable Alarm
50					Read Configurable Alarm
64	✓		✓	✓	Receiver Signal Monitor Average Optical Power
66	✓		✓	✓	Transponder Temperature Monitor
6B	✓		✓	✓	Receiver Signal Monitor Average Optical Power (in dBm)
81	✓		✓	✓	Read RX Alarm Status Register
82	✓		✓	✓	Read Power Alarm Status Register
83	✓		✓	✓	Set Rx Interrupt Alarm Mask Register
84	✓		✓	✓	Read Rx Interrupt Alarm Mask Register
87	✓		✓	✓	Set Power Supply Alarm Mask Register
88	✓		✓	✓	Read Power Supply Alarm Mask Register
89	✓		✓	✓	Read Summary Alarm Register
8A	✓		✓	✓	Interrupt Control
A0	✓		✓	✓	Read Supplier Identifier Code

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A1	✓		✓	✓	Read Module Type Code
A2	✓		✓	✓	Read Customer Parameters
A3	✓		✓	✓	Write Customer Parameters
A7	✓		✓	✓	Read Revision Codes
A8	✓		✓	✓	Read Unit Serial Number
A9	✓		✓	✓	Read Unit Manufacture Date
AA	✓		✓	✓	Read Unit Part Number
C0	✓		✓	✓	Read Link Status
C1	✓	🔒	✓	✓	Enter Pin Control Mode
C2	✓		✓	✓	Read Maximum I2C Rate
C3	✓		✓	✓	Enter Protected Mode
C4	✓		✓	✓	Exit Protected Mode
C5	✓		✓	✓	Reset CPN
C7	✓		✓	✓	Read Edition and Mode
F0 to FF		🔒🔒	✓	✓	Supplier Reserved Codes

7 Mechanical Specifications

The mechanical dimensions of this module is shown in Figure 3

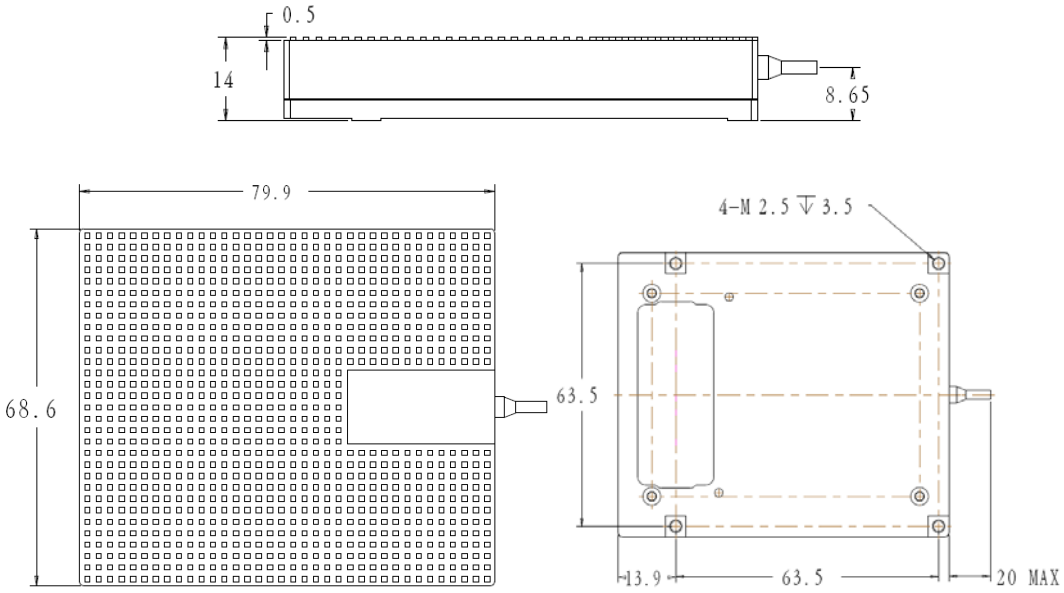

Figure 3 Mechanical Dimensions

Table 14 specifies the fiber and fiber connector for GR3T1LL, for applications, a configuration of the optical connector should be supported.

Table 14 Fiber Connector Type

Parameter	Specification	Units
Fiber pigtail	0.9mm diameter tight buffer fiber	
Length	1.0	m
Minimal Radius	30	mm
Connector	Straight/Angled LC/PC	

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8 Order Information

Table 15 Order Information

Part Number	Application	Date Rate	Fiber Type	Mechanical
GR3T1LL	40Gb/s VSR RX	STM256/ OTU3	LC/PC	LFF

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Contact

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